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~~41~~. (Amended) The high bandwidth processor interface defined in claim 6 ~~38~~, wherein the plural bits comprise eight input bits [of data] and eight output bits.

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~~42~~. (Amended) The high bandwidth processor interface defined in claim 6 ~~38~~, wherein the [paired links each further comprise] high bandwidth data channel further comprises termination resistors to form matched impedances for each of the plural bits of data [paired link].

R E M A R K S

I. INTRODUCTION

In response to the Office Action Applicants have amended the title to be more clearly indicative of the invention to which the claims are directed. Applicants have also amended claims 33, 34, 36, and 38-42, to recite limitations whereby a cache within the high bandwidth processor interface is configured to transmit and receive memory access requests and memory access responses in the form of packets comprising command information, address information, and data. The command information includes identification data for linking the memory access responses to respective memory access requests. Applicants respectfully submit that, based on the reasons that follow, amended claim 33, along with claims 34-43 dependent therefrom, are patentable over United States Patent No. 5,201,056 to Daniel et al. ("the '056 patent").

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II. THE PRESENT INVENTION IS PATENTABLE OVER THE '056 PATENT BECAUSE THE '056 PATENT LACKS ANY DISCLOSURE OR SUGGESTION OF A CACHE, AS RECITED IN CLAIM 33, AND OF A DIFFERENTIAL HIGH BANDWIDTH DATA CHANNEL COMPRISING UNIDIRECTIONAL PORTS, AS RECITED IN CLAIM 38

The Office Action rejects claims 33-43 under 35 U.S.C. § 103(a) as being unpatentable over the '056 patent.

Claim 33 claims a high bandwidth processor interface for receiving and transmitting a media stream. The high bandwidth interface includes a cache that transmits and receives media information consisting of memory access requests and memory access responses. The cache is configured to transmit and receive the media information in the form of packets comprising command information, address information, and data. The command information includes identification data for linking the memory access responses to respective memory access requests. The high bandwidth interface thereby enables a processor to issue multiple requests, the number of which depending on the number of bits allocated to the identification data, to each of a multiple number of memory devices. The processor then links each of the memory access responses, received in response to the various outstanding requests, to the associated request according to the identification information contained in the response. Further, the high bandwidth interface provides for a serial bus configuration that maintains data transfer rates in the gigabyte per second range, and eliminates the need for bus arbitration circuitry and processing.

The '056 patent discloses a RISC microprocessor architecture that includes a tag extension on full precision 32 bit data and instruction words. The tag extension provides instruction dependent control bits that are set and tested for control of program execution and branching dependent on the test results, and bits for identification of the data and/or instruction type. The '056 patent, however, lacks any disclosure or suggestion of a processor interface that comprises a cache configured for transmission and receipt of memory access requests and responses in the form of packets, as presently claimed.

Further, with regard to claim 38, the data channel of the claimed high bandwidth processor interface comprises unidirectional ports having differential data inputs and outputs and a differential clock signal for transmitting and receiving plural bits of data comprising the media stream. The '056 patent lacks any disclosure of such a configuration for the data port of the disclosed RISC processor.

The Office Action further asserts that,

> it would have been obvious to one of ordinary skill in the art at the time of invention to modify Daniel's system such that the transmission of the media information is performed at substantially peak rate during the system operation because it would have allowed the system to perform the data transfer operations at much higher rate based on the system requirements, thereby increasing the overall data transfer rate of the system and hence increase the overall performance of the system.

(Office Action, ¶ 22). Applicants respectfully traverse this assertion because the "sustained peak rates" of the data path as

recited in amended claim 33 and 36 refer to the data path to be interfaced with a media processor (as claimed in claim 36), and not the I/O data channel of the high bandwidth processor interface. The sustained peak rates of the data path are achieved by a media processor to be interfaced with the data path, and that media processor dynamically partitions a plurality of data streams concurrently transmitted over the data path and processes those data streams in parallel. The high bandwidth interface presently claimed, as presented above, provides an architecture that enables a processor to simultaneously issue multiple requests to each of a multiple number of memory devices. Accordingly, as presented above, claim 33 recites a novel architecture that provides inventive steps beyond a mere speed increase over the invention disclosed in the '056 patent.

Therefore, Applicants submit that claim 33 is patentable over the '056 patent. Additionally, Applicants submit that claims 34-43, being dependent from patentable base claim 33, are also patentable over the '056 patent.

Accordingly, Applicants respectfully request that the § 103(a) rejection of claims 33-43 be withdrawn.

III. CONCLUSION

Having completely responded to the Office Action, Applicants submit that all pending claims are in condition for allowance, an indication for which is respectfully solicited..

Respectfully submitted,

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